ABSTRACT:

This paper focus on techniques aimed at decreasing the power loss by the network links. In fact, the power loss by the network links is as equal as that loss by routers and network interfaces (NIs) and their difference is expected to increase as technology scales. As technology shrinks, the power loss by the links of a network-on-chip (NoC) starts to release with the power loss by the other aim of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper, we present a set of data encoding techniques aimed at reducing the power loss by the links of an NoC. The proposed work is general and clear with respect to the essential NoC fabric.

Index Terms—Coupling switching activity; data encoding; interconnection on chip; low;

1. Introduction

Network on chip is an emerging approach for the design of on chip communication architecture. A network on chip communication gives resistance in the topology, in support to that the flow control, advance routing algorithms, self switching techniques guaranteeing the quality of service. System on chip is an departure to design the communication system between property cores in a system. The communication in system on chip uses dedicated buses between communicating resources. This will not give any resistance since the needs of the communication, in each case, have to be thought of every time a design is made.

2. Overview of Proposal

The basic concept is to apply the encoding technique in end-to-end links in resource network interface of wormhole routed network on chip. The most suitable switching technique for on chip communication is wormhole switching.

Figure 1. General Scheme of proposed approach

The channel nature is the basic concept for the wormhole switching. The links of the routing path are crossed by the same interruption of flits, the encoding technique ensure the same switching behavior in each routing path. The encoder and decoder blocks are incorporated in the network interface. The encoder encodes the outgoing flit in the packet in such a way that the power dissipated in minimized by inter router point to point links which form the routing path.

3. PROPOSED ENCODING SCHEMES
In this section, we present the proposed encoding techniques whose goal is to decrease power loss by minimizing the coupling transition activities on the links of the interconnection. Let us first explain the power model that contains different components of power loss of a link. The dynamic power lossed by the interconnects and drivers is

\[ P = [T0→1 (Cs + Cl ) + TcCc] V2ddFck \]

Where \( T0→1 \) is the number of \( 0 \rightarrow 1 \) transitions in the bus in two consecutive transmissions, \( Tc \) is the number of correlated switching between physically adjacent lines, \( Cs \) is the line to substrate capacitance, \( Cl \) is the load capacitance, \( Cc \) is the coupling capacitance, \( Vdd \) is the supply voltage, and \( Fck \) is the clock frequency. The effective switched capacitance varies from type to type, and hence, the coupling transition activity, \( Tc \), is a weighted sum of different types of coupling transition contributions. Therefore

\[ Tc = K1T1 + K2T2 + K3T3 + K4T4 \]

Where \( Ti \) is the average number of Type \( i \) transition and \( Ki \) is its corresponding weight. We use \( K1 = 1, K2 = 2, and K3 = K4 = 0 \). The occurrence probability for a random set of data is 1/2 and 1/8, respectively. This leads to a higher value for \( K1T1 \) compared with \( K2T2 \) suggesting that minimizing the number of transition may lead to a considerable power loss. Using (2), one may express (1) as

\[ P = [T0→1 (Cs + Cl ) + (T1 + 2T2) Cc] V2ddFck \]

According to [3], \( Cl \) can be neglected

\[ P \propto T0→1Cs + (T1 + 2T2)Cc \]

Consider that flit \((t-1)\) and flit \((t)\) refer to the previous flit which was transferred via the link and the flit which is about to pass through the link, respectively. Note that the first bit is the value of the generic \( i \)th line of the link, whereas the second bit represents the value of its \((i+1)\)th line. In the rest of this section, we present three data encoding techniques designed for reducing the dynamic power loss of the network links along with a possible hardware implementation of the decoder.

**A. Scheme I**

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

**I) Power Model:** If the flit is odd inverted before being transmitted, the dynamic power on the link is

\[ P_0 \propto T_0→1+ K1T_1+ K2T_2+ K3T_3+ K4T_4Cc \]

where \( T_0→1, T_1, T_2, T_3, \) and \( T_4 \), are the self-transition activity, and the coupling transition activity of Types I, II, III, and IV, respectively. Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted as is and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic \( i \)th line of the link, whereas the second bit represents the value of its \((i+1)\)th line. For each partition, the first (second) line represents the values at time \( t = 1 \) (0). As Table I shows, if the flit is odd inverted, Types II, III, and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as \( T_1^*, T_1^{**}, \) and \( T_1^{***} \) in the table convert to Types II, III, and IV transitions, respectively. Also, we have \( T_0→0= T0→0(od) + T0→1(even) \) where odd/even refers to odd/even lines. Therefore, (5) can be expressed as

\[ P_0 \propto _T0→0(od) + T0→1(even)Cs + [K1 (T2+T3+T4)+K2T_1^{***}+K3T_1^{*}+K4T_1^{**}]Cc \]

(6)
Thus, if $P > P_\text{c}$, it is convenient to odd invert the flit before transmission to reduce the link power dissipation. Using (4) and (6) and noting that $Cc/C_s = 4$ [26], we obtain the following odd invert condition

$$1/4T_0 \rightarrow 1 + T_1 + 2T_2 > 1/4 \cdot T_0 \rightarrow 0 \ (\text{odd}) + T_0 \rightarrow 1 \ (\text{even}) + T_2 + T_3 + T_4 + 2T_1 \ ***$$

which is the exact condition to be used to decide whether the odd invert has to be performed. Since the terms $T_0 \rightarrow 1 \ (\text{odd})$ and $T_0 \rightarrow 0 \ (\text{odd})$ are weighted with a factor of 1/4, for link widths greater than 16 bits, the misprediction of the invert condition will not exceed 1.2% on average [23]. Thus, we can approximate the exact condition as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1 \ *** \ \ldots \ldots \ (8)$$

Of course, the use of the approximated odd invert condition reduces the effectiveness of the encoding scheme due to the error induced by the approximation but it simplifies the hardware implementation of encoder. Now, defining

$$T_x = T_3 + T_4 + T_1$$

and

$$T_y = T_2 + T_1 - T_1 \ *** \ \ldots \ldots \ (9)$$

one can rewrite (8) as

$$T_y > T_x \ \ldots \ldots \ (10)$$

Assuming the link width of $w$ bits, the total transition between adjacent lines is $w - 1$, and hence

$$T_y + T_x = w - 1 \ \ldots \ldots \ (11)$$

Thus, we can write (10) as

$$T_y > (w - 1)/2 \ \ldots \ldots \ (12)$$

This presents the condition used to determine whether the odd inversion has to be performed or not.

**B. Scheme II**

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.
Power Model: Let us indicate with $P$, $P^1$, and $P^{11}$ the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when $P^1 < P^{11}$ and $P^1 < P$. The power $P^{11}$ is given by

$$P^{11} \propto T_1 + 2T_4 \quad \cdots \cdots \quad (13)$$

Neglecting the self-switching activity, we obtain the condition $P^1 < P^{11}$ as [see (7) and (13)]

$$T_2 + T_3 + T_4 + 2T_1 \quad \cdots \cdots \quad (14)$$

Therefore, using (9) and (11), we can write

$$2(T_2 - T_4 \quad \cdots \cdots) < 2Ty - w + 1 \quad \cdots \cdots \quad (15)$$

Figure 3. Encoder architecture Scheme II.

Based on (12) and (15), the odd inversion condition is obtained as

$$2(T_2 - T_4 \quad \cdots \cdots) < 2Ty - w + 1 \quad \cdots \cdots \quad (16)$$

Similarly, the condition for the full inversion is obtained from

$$P^{11} < P \quad \text{and} \quad P^{11} < P^1$$

The inequality $P^{11} < P$ is satisfied when [23]

$$T_2 > T_4 \quad \cdots \cdots \quad (17)$$

Therefore, using (15) and (17), the full inversion condition is obtained as

$$2(T_2 - T_4 \quad \cdots \cdots) > 2Ty - w + 1 \quad T_2 > T_4 \quad \cdots \cdots \quad (18)$$

When none of (16) or (18) is satisfied, no inversion will be performed.

C. Scheme III

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I ($T \quad \cdots \cdots 1$) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as $T \quad \cdots \cdots 1$ in the table are converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

1) Power Model: Let us indicate with $P^1$, $P^{11}$, and $P^{111}$ the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, full inversion, and even inversion, respectively. Similar to the analysis given for Scheme I, we can approximate the condition $P^{111} < P$ as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1 \quad \cdots \cdots \quad (19)$$
Defining

\[ Te = T2 + T1 - T1^* \] (20)

we obtain the condition \( p^{111} < p \) as \( Te > (w-1)/2 \) (21).

Similar to the analysis given for scheme II, we can approximate the condition \( p^{111} < p \) as

\[ T2 + T3 + T4 + 2T1^* < T2 + T3 + T4 + 2T1^* \] (22)

Using (9) and (20), we can rewrite (22) as

\[ Te > Ty \ldots \ldots \ldots (23) \]

Also, we obtain the condition \( p^{111} < p^{11} \) as [see (13) and (19)]

\[ T2 + T3 + T4 + 2T1^* < T1 + 2T4^* \] (24)

Now, define

\[ Tr = T3 + T4 + T1^* \]

and

\[ Te = T2 + T1 - T1^* \] (25)

Assuming the link width of \( w \) bits, the total transition between adjacent lines is \( w-1 \), and hence

\[ Te + Tr = w - 1 \ldots \ldots (26) \]

Using (26), we can rewrite (24) as

\[ 2 (T2 - T4^*) < 2Te - w + 1 \ldots \ldots (27) \]

The even inversion leads to power reduction when \( p^{111} < p, p^{111} < p^l \), and \( p^{111} < p^{11} \). Based on (21), (23), and (27), we obtain

\[ Te > (w-1)/2, Te > Ty, 2(T2 - T4^*) < 2Te - w + 1 \ldots \ldots (28) \]

The full inversion leads to power reduction when \( p^{111} < p, p^{111} < p^l \), and \( p^{111} < p^{11} \). Therefore, using (18) and (27), the full inversion condition is obtained as

\[ 2 (T2 - T4^*) > 2Ty - w + 1, (T2 > T4^*)2 (T2 - T4^*) > 2Te - w + 1 \ldots \ldots (29) \]

Similarly, the condition for the odd inversion is obtained from \( p^l < p, p^l < p^{11} \), and \( p^l < p^{11} \). Based on (16) and (23), the odd inversion condition is satisfied when
2 \left( T_2 - T_4 \right) < 2T_y - w + 1, \quad T_y > (w - 1) / 2T_e < T_y \quad \ldots (30)

When none of (28), (29), or (30) is satisfied, no inversion will be performed.

4. Simulation Results
FIG: WAVEFORMS FOR SCHEME-II

FIG: WAVE FORMS FOR SCHEME-II

FIG: RTL SCHEMATIC DIAGRAM FOR SCHEME-III

FIG: WAVE FORMS FOR SCHEME-III
Conclusions

The Encoding techniques to reduce power consumption due to self switching activity and cross coupling in NoC links. The encoding technique which allows reducing the power dissipated by the links of a NoC and contributed by both the self switching activity and the coupling switching activity. The proposed encoding technique has two stages 1st stage reduce the self switching and the second stage is designed so to reduce the cross coupling activity. The encoder and decoder is simulated for the different data stream .The significant amount of power reduction is obtained from the encoding technique; the no. of LUTs required is also less but the other parameters such as delay is increased.

Most of power is dissipated by links, routers and network interface. In all the papers they focused on the power reduction by using encoding technique. The novel encoding technique reduced power 17.34%, the result of novel encoding is compared with BI encoding. The power reduction of novel encoding is better than the BI encoding. SCDBI encoding reduced power 34.67% and area is 8%. But data encoding is more effective as it gives 51% power reduction and also 14% of energy consumption [4].The proposed scheme gives the advanced architecture with general and transparent with respect to the underlying NoC fabric. It has achieved the effectiveness of the proposed schemes which allows reducing 57% power dissipation and saves 26% area with the significant minimum delay that is 7.948ns and gives the 0.035J energy consumption.

Reference


Guide details:


