Design of High Speed Hybrid Sqrt Carry Select Adder

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ABSTRACT

Power dissipation is one of the most important design objectives in integrated circuits, after speed & area. As adders are the most widely used components in such circuits, design of efficient adder is of much concern for researchers. This paper presents performance analysis of different Fast Adders. The comparison is done on the basis of three performance parameters i.e. Area, Speed and Power consumption. We present a modified carry select adder designed in different stages. Results obtained from modified carry select adders are better in area and power consumption in comparison with Regular CSA, BEC-CSA, CBL-CSA. The design has been synthesized at 90nm process technology targeting using Xilinx 14.7.

I. INTRODUCTION

Performance of large digital circuits is dependent on the speed of circuits that form various functional units. Adders are one of the widely used in digital integrated circuit and system design. High speed adder is the necessary component in a data path, e.g. Microprocessors and a Digital signal processor. For adding two binary numbers there exists several adder structures based on very different design ideas. Thus if one need to implement an addition circuit one must decide which circuit is most appropriate for its planned application. There are many binary adder architecture ideas to be implemented in such applications. However, it has been difficult to do well both in speed and in area. The easiest type of parallel adder to build is a ripple carry adder, which uses a chain of one bit full adder to generate its output. The Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but lead to increase in area. The Carry Select Adder (CSA) provides a compromise between small areas but longer delay Ripple Carry Adder (RCA) and a larger area with shorter delay Carry Look-Ahead Adder (CLA).

In mobile electronics, reducing area and power consumption are key factors in increasing portability and battery life. Even in servers and desktop computers, power consumption is an important design constraint. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Among various adders, the CSA is intermediate regarding speed and area.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers (mux). The existing modified SQRT CSLA is to use Binary to Excess-I Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption with slightly increase in the delay. The basic idea of the proposed architecture is that which replaces the BEC by Common Boolean Logic.

In this paper, an area-efficient carry select adder by sharing the common Boolean logic term is proposed. After Boolean simplification, it can remove the duplicated adder cells in the conventional carry select adder. It generates a duplicate sum and Carry-out signal by using NOT and OR gate and select value with the help of multiplexer. The multiplexer is used to select...
the correct output according to its previous carry-out signal. This paper is organized as follows: Section II and section III explains the regular and modified CSLA and detail structure of BEC respectively. A section IV deals with Common Boolean Logic (CBL) and section V explain about the proposed architecture. Comparisons of area, power and delay Results are analyzed in the section VI. Section VII concludes.

II. BASIC STRUCTURE OF REGULAR SQRT CSLA.

The basic square root Carry select adder has a dual ripple carry adder with 2: 1 multiplexer the main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The regular 16-bit Carry select adder is shown in Fig. 1.[7]. It is divided into five groups with different bit size RCA. From the structure of Regular CSLA, there is scope for reducing area and power consumption. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer [1]. Internal structure of the group 3 of regular 16-bit CSLA is shown Fig.2. By manually counting the number of gates used for group 3 is 87 (full adder, half adder, and multiplexer) and 13ns delay. One input to the mux goes from the RCA with Cin=O and other input from the RCA with Cin=1.

III. MODIFIED SQRT CSLA USING BEC

The modified Carry select adder has a single ripple carry adder with Binary to Excess-I converter, which replace the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+ 1-bit BEC is required. A structure and the function table of a 4-b BEC is shown in Table I, respectively. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, I\xOR).

<table>
<thead>
<tr>
<th>Binary [3:0]</th>
<th>Excess-I [3:0]</th>
</tr>
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<tbody>
<tr>
<td>0000</td>
<td>0001</td>
</tr>
<tr>
<td>0001</td>
<td>0010</td>
</tr>
<tr>
<td>1110</td>
<td>1111</td>
</tr>
<tr>
<td>1111</td>
<td>0000</td>
</tr>
</tbody>
</table>

The modified 16-bit CSLA using BEC is shown in Fig.5. The structure is again divided into five groups with different bit size RCA and BEC. The group 3 of the modified 16-bit CSLA is shown Fig. 6. By manually counting the number of gates used for group 3 is 61 (full adder, half adder, multiplexer, BEC) and the delay is 16ns. The parallel RCA with Cin= 1 is replaced with BEC. One input to the multiplexer goes from the RCA with Cin=O and other input from the BEC.
Comparing the group 3 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

IV. COMMON BOOLEAN LOGIC

In proposed work, an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. In this way, it save many transistor counts and achieve a low Power. Through analyzing the truth table of a single-bit full adder, To find out that the output of summation signal as carry-in signal is logic "0" is the inverse signal of itself as carry-in signal is logic "1". As illustrated as two dotted circles in the truth table of Fig. 7. By sharing the common Boolean logic term in summation generation, a proposed carry select adder design is illustrated in Fig. 8. To share the common Boolean logic term, it only needs to implement one OR gate with one INV gate to generate the Carry signal and summation signal pair.

Once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal.

As compared with the Modified Carry Select adder, the proposed CSLA is little bit faster, but the speed is nearly equal to the Regular CSLA. The delay time in our proposed adder design is also proportional to the bit number N; however, the delay time of multiplexer is shorter than that of full adder. The Proposed CSLA is Area efficient & low power, but the speed equal to the Regular CSLA.

V. PROPOSED CSLA ARCHITECTURE

This method replaces the BEC add one circuit by Common Boolean Logic. The output waveform of full adder for carry in signal is '1' is generating summation and carry signal by just using a TNV and OR gate. It is shown in fig. 9

The Summation and carry signal for FA which has Cin=1, Generate by INV and OR gate. Through the
multiplexer, we can select the correct output result according to the logic state of carry-in signal.

Internal structure of the group 3 of Proposed CSLA is shown Fig. 10. By manually counting the number of gates used for group 3 is 36 (full adder, half adder, and multiplexer, not, or gate). One input to the mux goes from the RCA block with Ci=0 and other input from the CBL.

The Group 3 performed a three bit addition which are A with B, A[S] with B[S] and A with B. This is done by I halfadder (RA) and two full adder (FA). The CBL block has a 4:2 multiplexer to select the appropriate carryout and summation signal for Carry-in signal '1'. Through 2:1 multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexer and 4:2 multiplexer is the combination of 2:1 multiplexer.

VI. COMPARSTONS OF ADDERS

The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit SQRT CSLA is done by cascading the two 16-bit SQRT CSLA. Table II exhibit the delay and area of regular, modified and proposed 16-bit SQRT CSLA. Simulation is carried out using Xilinx simulation tool and Spartan 3E as the target device. The major disadvantage of modified architecture using BEC is increasing area. This disadvantage is overcome in the proposed architecture which reduces area than the regular and modified Square-root Carry select adder. The comparison chart between area, delay and logic levels is shown below.

VII Results

Fig: 16-bit SQRT CSLA-CBL(AREA)

Fig: 16-bit SQRT CSLA-CBL (DELAY)

VIII CONCLUSION

The 8-bit SQRT CSLA is done by the same structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are directly In this paper, an area efficient square-root carry select adder is proposed. By sharing the common Boolean logic (CBL) term, the duplicated adder cells in the conventional carry select adder is removed.

The reduced number of gates of this work offers the great advantage in the reduction of area. The regular SQRT CSLA has the disadvantage of occupying more chip area. This paper proposes a scheme which reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 64 and 128 bit SQRT CSLA.

References


