An Efficient Design of CMOS Full Adder Low Power High Speed

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Abstract-
The full Adder is designed using CMOS logic style by dividing it in three modules so that it can be optimized at various levels. First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. The main motive is to determine the comparison of power, surface area and complexity of Full adder designs using CMOS Logic Styles. Logic style affects the switching capacitance, transition activity, short circuit current and delay. Various logic styles have been compared taking full adder as a reference circuit and power dissipation and delay as reference parameters. Full adder Design is better compared to conventional design. Transistor Design with respect to power, delay, Power Delay Product Comparison. It is observed that less power is consumed in the Transmission based full adder than the Convention full adder and Pass Transistor full adder.

Keywords- CMOS logic style; full adder; high speed; low power

1. INTRODUCTION

Full adder is a basic building block for various arithmetic circuits such as multipliers, compressors, comparators and so on. The power requirement and output delay of these circuits is greatly depending upon the power requirement and delay of the full adder circuits. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. So for designing the high performance arithmetic circuits, minimization of the power and delay of the full adder circuit is required. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. Multipliers are the key elements in several Computer Arithmetic circuit applications like Image and video Processing, Multimedia like in Oscillators and Microprocessors like in ALUs, Multiplier and accumulator units, Digital Signal Processors like in Filter designing, convolutes etc.,. In most of the VLSI systems, multiplier lies in the critical path directly. The performance of multipliers helps in influencing the performance of several DSP algorithms and processor’s running speed. Computational and market demands have driven VLSI microprocessors to double their performance every three years. A good circuit design and choice of appropriate logic style is equally important in achieving this performance goal. Power and area consumption are two important considerations for VLSI system designer engineers. The designers are now focusing on multipliers of high speed and at the same time maintaining low power consumption and further to have low power delay product.

Several logic styles for designing the Full adder have been proposed. In classical design of full adder normally single CMOS structure is used for the whole design, Such as the standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full swing output and good driving capabilities but the main drawback of this circuit is high input capacitance and use of large no. of PMOS, due to which the speed of this structure is degraded. In another conventional design the complementary pass transistor logic (CPL) is used, which provides good driving capability, full swing of operation and high speed, but its main disadvantage is high power dissipation due to large number of internal nodes in the cell. Designing an Arithmetic Unit at a particular circuit level effects its...
performance as various performance determining factors such as switching capacitance, transition activity and short circuit current are strongly influenced by chosen logic style. The speed of dynamic CMOS logic style adder is higher. It has several demerits such as charge sharing, high clock load, higher switching activities and lower noise immunity and it requires high power for driving the clock lines. Another logic styles are transmission-gate full adder (TGA) and transmission-function full adder (TFA) based upon transmission gates and transmission function theory. These full adders are very low power consuming, but have very low driving capabilities. In order to optimize the reduction phase, compressors can be used for partial product accumulation. Column Compression (CC) is the technique used to reduce the power consumption and delay in multiplier design, in which the compressors used in multipliers are accumulated with partial products column–wise.

"CMOS" refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. CMOS logic design style uses more than one module for designing of full adder. In this design style full adder structure is designed by breaking the full adder into three modules. Module I is an XOR-XNOR circuit which drives the other modules, So it must have good driving capability and provide full swing outputs simultaneously. Module II and Module III are the sum and carry circuits which use the output of first module and third input signal as input to produce the sum and carry outputs respectively. General structure of hybrid CMOS design style is shown in Fig.1. General structure of hybrid CMOS design style is shown in fig.1. This logic design style provides the freedom to take the optimum circuits for every module for getting the optimum performance of adder cell. These adders generally lack the driving capabilities. Their performance as a single bit is good, but as the size of chain increases, the performance degraded drastically. But in this paper we tried to present an adder cell with this logic style for which the performance is not degraded in adder chain. We tried to get better delay performance from Cin to Cout and evaluate the performance of adder cell in 4 bit adder chain and 8 bit adder chain.

![Fig.1. General Form of CMOS logic design](image)

2. CMOS LOGIC DESIGN

Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synpaper algorithms, from register transfer level (RTL) down to gate level and net list.

2.1 CMOS Technology:
Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS is also sometimes referred to as complementary-symmetry metal–oxide semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor.
The sum (S) and carry (Cout) expression for a 1-bit full adder with three binary inputs A, B and Cin are given by

\[ S = A \oplus B \oplus C_{in} \]
\[ C_{out} = A \cdot B + C_{in} \cdot (A \oplus B) \]

In CMOS architecture, we get XOR and XNOR of A and B inputs as the intermediate signal at the output of module I. These input signals and Cin are available for the input of module II and module III. So we get new expression for sum and carry using XOR output H and XNOR output H'.

\[ S = H \oplus C_{in} = H \cdot C_{in} + H' \cdot C_{in} \]
\[ C_{out} = H' \cdot A + H \cdot C_{in} \]

Static CMOS type of XOR-XNOR module uses both pMOS and nMOS transistors and it consumes large amount of power and many transistors and so larger area. Static XNOR-XOR also uses Complementary CMOS style of pull-up and pull-down transistors, but it also has large power consumption and not used at low voltages. A XOR-XNOR gate with feedback transistors is suitable at low voltages but the input load is doubled, and this causes slow response if cascaded, and area increased. To have high speed performance than the earlier three types of XOR-XNOR gates, it is convenient to use the XOR-XNOR module as shown in Fig.2. It can operate well at low supply voltages and it uses only 8 transistors. It also provides good driving capability.

Fig.2. Circuit diagram of XOR-XNOR

2.2 CMOS Process Enhancements:
1) Silicon on Insulator:
As the name suggests transistors are fabricated on an insulator (SiO2 or sapphire) Insulating substrate eliminates capacitance between the source/drain and body, higher speed devices and low leakage currents.
2) Transistors:
Multiple threshold voltages and oxide thicknesses Processes offer multiple threshold voltages Low threshold devices: faster, higher leakage. High threshold devices: opposite Thin oxides: provide high ON currents but cannot handle high voltages. dielectrics Transistors need high gate capacitance to channel Thin gates and therefore high gate leakages Thicker gates that leak less can be made with high-k materials e.g. hafnium oxide (k=20), zirconium oxide (k=23), silicon nitride (k=6.5-7.5) Applied using ALD, MOCVD (metal–organic CVD) or sputtering.
2.3 Design and Architecture of Full Adder:

The ultimate goal of a binary full-adder (BFA) is to implement the following truth table for each bit:

<table>
<thead>
<tr>
<th>$C_{in}$</th>
<th>A</th>
<th>B</th>
<th>SUM</th>
<th>$C_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td>1</td>
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<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1. Truth table adder design

Logically, carry = $AB + BC + CA$ and $SUM = C\oplus B\oplus A$, where $k$ is an integer 0 to $n$ for an $n$-bit adder. Generally, adders of $n$-bits are created by chaining together $n$ of these 1-bit adder slices.

3. EXISTING SYSTEM DESIGN

Digital schematic is designed using DSCH for full adder using 28 transistors which occupies a lot of surface area and power consumed is also high which can be reduced by reducing number of transistors. The complexity can be decreased by modifying this existing full adder design.

The twenty eight bit transistor based on regular CMOS structure i.e. pull-up and pull-down network. One of the most significant advantages of this full adder waist high noise margins and thus reliable operation at low voltages. The layout of CMOS gates was also simplified due to the complementary transistor pairs. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.
Here implementation of the full adder circuit is designed by taking the logic equations and translate them directly into complementary CMOS circuit in fig. . Some logic manipulations can help to reduce the transistor count. For instance, it is advantageous to share some logic between the sum and carry – generation sub circuits, as long as this does not slow down the carry generation, Which is the most critical part as stated previously. The following is an example of Such as reorganized equation set:

\[ C_{out} = A.B + B.C_{in} + A.C_{in} \]
\[ S = A.B.C_{in} + C_{out} \cdot (A + B + C_{in}) \]

The equivalence with the original equations is easily verified. The corresponding adder design, using complementary static CMOS, is shown in figure and the gate level implementation is shown in figure. The transistors of the circuit produce the Cout and the remaining transistors produce the Sum outputs. Therefore the delay for computing Cout is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area.

**4. POWER DISSIPATION**

There are three sources of power dissipation viz. static power, dynamic power and short circuit power dissipation. Static power dissipation is associated with leakage current and can be improved with the advancement in fabrication technology only. Dynamic power dissipation is given by the following equation:

\[ P_d = \alpha C_L V_{DD}^2 f_{CLK} \]

Where \( \alpha \) is the switching activity, is the load capacitance, VDD is the supply voltage and fCLK is the clock frequency.

Other source of power dissipation is short circuit power dissipation that arises when direct current flows from VDD to ground. Short circuit power dissipation, depends on rise time and fall time because it is only during transition that transistors between VDD and ground remains on and short circuit power dissipation comes into play. In the optimized full adder circuit, both transistor count and area has been reduced that lowers the dynamic power dissipation as well as short circuit power dissipation and hence the total power dissipation reduces.

<table>
<thead>
<tr>
<th>Circuit (Full Adder)</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>180 nm</td>
<td>3.998 E-6</td>
</tr>
<tr>
<td>CMOS Full Adder</td>
<td>1.519 E-6</td>
</tr>
<tr>
<td>TG Full adder</td>
<td>1.823 E-6</td>
</tr>
</tbody>
</table>

Table 2. Comparison among various Adders

**SIMULATION ENVIRONMENT**

Figure 5 shows the test used for the analysis of the full-adders. This simulation is used for comparing the full-adders analyzed in [9], [14], with the addition of the inverters at the outputs. The size of the input buffers experience some degradation in the input signals. The size of the output buffers equals the load of four small inverters. This test is presented as a static CMOS gate for driving the full-adder cell under test. The benefit of using this simulation is less power consumption. The short-circuit power consuming inverters are connected to the device under test (DUT) inputs. This power consumption varies as per the capacitive load that the DUT offers at the inputs. The energy required to charge and discharge the DUT internal nodes when the module has no direct power supply connections, comes through these inverters connected at the DUT inputs.
Figure 5: Shows the test used for the analysis of the full-adders

Figure 5: Test bed used for simulating the full-adders under comparison the short-circuit consumption of the DUT on its own, receives signals with finite slopes coming from the buffers are connected at the inputs, instead of ideal ones coming from voltage sources. The short-circuit and static power consumption of the inverter connected to the outputs of the DUT, which are because of the finite slopes and degraded voltage swing of the full-adder output signals. The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the DUT comes from the fact that the DUT is always be used in combination with other devices to build a larger system. These static inverters are a good generalization for any operating scenario to be considered. For the stimulus vectors, we used the test inputs patterns as recommended in 1-bit CMOS adder, as they exercise all the input combinations necessary to determine the propagation delay and power consumption.

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5. CONCLUSION

Using CMOS logic design style the designer can able to select the various modules in a circuit depending upon the application. Using the adder categorization and CMOS design style, many full adders can be designed. The circuit uses the XOR-XNOR gate which provides good driving capability, high speed and low power. The CMOS full adder has better performance than most of the standard full-adder cells owing to the novels design modules. Also it has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices is considered to be the most energy-efficient solution for low-performance applications. It performs well with supply voltage ranging from 1.2V to 2.4V. When embedded in a parallel adder chain, it outperforms all the other adders making it suitable for larger arithmetic circuits. Hence reduced complexity is achieved by using less number of transistors. Also power is reduced up to 30% in comparison to conventional design.

6. REFERENCES


