ABSTRACT: Low power design has been an important part in VLSI system design. Digital multipliers are most critical functional units of digital filters. The overall performance of digital filters depends on the throughput of multiplier design. Aging problem of transistors has a significant effect on performance of these systems and in long term, the system may fail due to delay problems. Aging effect can be reduced by using over-design approaches, but these approaches leads to area, power inefficiency. Moreover, timing violations occur when fixed latency designs are used. Hence to reduce timing violations and to ensure reliable operation under aging effect, low power variable latency multiplier with adaptive hold logic is used. This multiplier design can be applied to digital filter so as to enhance its performance. The VHDL language is used for coding, synthesis was done by using Xilinx ISE.

(1) INTRODUCTION

Filters are widely used in signal processing and communication systems. Digital finite impulse response (FIR) filters are the basic building block of many digital signal processing systems. In signal processing, the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as components lying within a certain frequency range. The main objectives of digital FIR filter are to filter out undesirable parts of the signal, shape the spectrum of signals in communication channels, signal detection or analysis in radar applications. An analog filter uses analog electronic circuits made up of components such as resistors, capacitors and operational amplifiers to produce the required filtering effect. Such filter circuits are widely used in such applications as noise reduction, videosignal enhancement, graphic equalizers in hi-fi systems, and many other areas. A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general-purpose computer, or a specialized DSP (Digital Signal Processor) chip. Digital filters are more advantageous when compared with analogones. Digital filters are easily designed, tested and implemented on a general purpose computer or workstation. Multiplication is an essential arithmetic operation for common DSP applications, such as filtering and fast Fourier transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP systems. The throughput of digital filter systems depends on these multipliers, and if these multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative bias temperature instability (NBTI) occurs when an nMOS transistor is under negative bias, resulting in aging effect. Aging effect degrades transistor speed by increase in threshold voltage, which results in real time delay problems. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. Traditional methods to reduce this aging effect were area and power inefficient [1].

Traditional circuits are based on fixed latency design. In fixed latency design, critical path delay as the overall circuit clock cycle in order to perform correctly. However, the probability that the critical path is activated is low. For these noncritical paths, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable-latency design was proposed to reduce the timing waste of traditional circuits. In variable-latency design, shortest paths are assigned to be executed within one cycle and longest paths within two or more cycle. When shorter paths are activated frequently, the average latency of variable-latency designs is better than that of fixed latency designs [1].

Main objective of the work is to design a digital filter using low power variable latency multiplier with AH logic. Low power variable latency multiplier is designed so as to ensure minimum performance degradation. The coding can be synthesized by the Xilinx ISE Design Suite.

(2) Methodology
Performance of digital filters depends on throughput of multipliers. The primary objective is power reduction with small area and delay overhead. Low power Variable latency multiplier design with AH logic introduces a multiplier, in which AHL circuit associated with it adjusts the circuit when timing delays occur so as to ensure minimum performance degradation.

2.1 Low Power Variable Latency Multiplier With AH Logic

The basic block diagram for low power variable latency multiplier with AH logic is shown in Figure 1, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column-bypassing multiplier, 2m 1-bit Razorflip-flops, and an AHL circuit. Clock is provided by the AND gate at the input.

The overall working of variable latency multiplier is as follows: when input patterns arrive, the column-bypassing multiplier and the AHL circuit execute simultaneously. Depending on the number of zeros in the multiplicand, the AHL circuit decides the number of clock cycles required for the current input pattern. If the input pattern requires two cycles to complete, the AHL will output 0 to disable the clock signal of the input flip-flops. Otherwise, the AHL will output 1 for normal operations.

In this paper, we propose an aging-aware reliable multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are summarized as follows:

1) Novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can decide whether the input patterns require one or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation after considerable aging occurs;

2) Comprehensive analysis and comparison of the multiplier’s performance under different cycle periods to show the effectiveness of our proposed architecture;

3) An aging-aware reliable multiplier design method that is suitable for large multipliers. Although the experiment is performed in 4- and 16-bit column multipliers, our proposed architecture can be easily extended to large designs;

(3) Proposed of Column-Bypassing Multiplier

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 2. The multiplier array consists of \((n-1)\) rows of carry save adder (CSA), in which each row contains \((n-1)\) full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation. The FAs in the AM are always active regardless of input states. In a low-power column-bypassing multiplier design, the corresponding bit in the multiplicand is 0. Fig. 3 shows a 4x4 column-bypassing multiplier. Supposing the inputs are 1010₂ * 1111₂, it can be seen that for the FAs in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product \(a_i b_i\). Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.
Hence, the FA is modified to add two tristate gates and one multiplexer. The multiplicand bit \( a_i \) can be used as the selector of the multiplexer to decide the output of the FA, and \( a_i \) can also be used as the selector of the tristate gate to turn off the input path of the FA. If \( a_i = 0 \), the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If \( a_i = 1 \), the normal sum result is selected. More details for the column-bypassing multiplier can be found.

**4) EXTENSION OF ROW MULTIPLIER**

A low-power row-bypassing multiplier [23] is also proposed to reduce the activity power of the AM. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing multiplier, but the selector of the multiplexers and the tristate gates use the multiplicator. Fig. 4 is a 4 × 4 row-bypassing multiplier. Each input is connected to an FA through a tristate gate. When the inputs are 11112 * 10012, the two inputs in the first and second rows are 0 for FAs. Because \( b_1 \) is 0, the multiplexers in the first row select \( a_i b_0 \) as the sum bit and select 0 as the carry bit. The inputs are bypassed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similarly, because \( b_2 \) is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row because \( b_3 \) is not zero. More details for the row-bypassing multiplier can also be found.

For example, Fig. 5 is an 8-bit variable-latency ripple carry adder (RCA). A8–A1, B8–B1 is 8-bit inputs, and S8–S1 are

![Fig. 5. 8-bit RCA with a hold logic circuit.](image)

**5) RESULTS**

The design entry is modeled using VHDL in Xilinx ISE Design with the project Starter Kit Board, to obtain the synthesis report. The simulation of the design is performed using XILINX 12.1. Structural model of fixed latency multiplier and low power variable latency multiplier with AH logic in Column 4x4, 16x16 is developed. The low power variable latency multiplier with AH logic contains modules such as a column bypassing multiplier, the razor flip-flop and an adaptive hold logic. The simulation results for the bypassing based multipliers are shown in Table 1.

Similarly in the case of delay, variable latency based multipliers has less delay when compared with fixed latency ones. Based on the circuit area, power and delay comparison, the 16x16 variable latency based multiplier with AH logic is the most efficient one and the 4x4 variable latency based multiplier with AH logic is the least efficient one. Hence, 16x16 variable latency multiplier with AH logic can be applied to digital FIR filter design so as to enhance its performance.
Low power utilization is the most important criteria for the high performance DSP system. High feat system can be achieved by reducing the dynamic power which in turn reduces the total power dissipation. Low power Variable-latency multiplier design with the adaptive hold logic is able to adjust the adaptive hold logic to mitigate performance degradation due to delay problems. Variable-latency design minimizes the timing waste of the noncritical paths. The Razor flip-flops detect the timing violations and re-execute the operations using two cycles. Variable-latency design can adjust clock cycle required by input patterns to minimize performance degradation. And hence variable latency multipliers have less performance degradation when compared with traditional fixed latency multipliers, which needs to consider the degradation by both the NBTI effect and use the worst case delay as the cycle period. Therefore, performance of digital FIR filters using low power variable latency multiplier with AH logic, can be enhanced by reduced delay, area and power.

REFERENCES


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