Design and Implementation of Five Level Inverter based MPPT Using Self Lift SEPIC Converter

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Abstract: The conventional power conditioning units require a DC-DC converter followed by an inverter circuit to deliver the required power to the load. This increases the required power conversion stages, system cost, size and reduces the overall system efficiency. Therefore, to maximize the efficiency of the renewable energy system, it is necessary to track the maximum power point of the input source. This paper presents the modeling and simulation of Incremental conductance (IncCond) Maximum Power Point Tracking (MPPT) using Multi level Single Ended Primary Inductance Converter (SEPIC) converter and compared its performance with self lift SEPIC converter. The solar panel model is developed using the basic circuit equations of photovoltaic cell. The MPP of a solar panel varies with irradiation and temperature. The IncCond algorithm is used to track the maximum power from the solar panel. The unregulated voltage from the panel will be regulated by using the Multi level SEPIC at the same time it can also supply the medium voltage and high voltage loads. The efficiency of the Multi level SEPIC converter over the self lift SEPIC converter has been tested by using Matlab/Simulink.

Index Terms— Microcontroller, Incremental conductance (IncCond) Maximum Power Point Tracking (MPPT), self lift SEPIC, photovoltaic (PV) system.

I. INTRODUCTION

According to the realization of high efficiency and low cost photovoltaic (PV) modules, interest in photovoltaic power generation system has increased over the past decade as aclean and infinite energy [1-2]. The PV modules have maximum operating points corresponding to the surrounding conditions such as intensity of the sunlight, the temperature of the PV modules, cell area, and load. When solar energy is used as apower source, the output power has to be maximized by improving the efficiency of the power conditioning equipment used and implementing parameters [3-7] of the module depend mainly on the solar irradiance and on the cells temperature, as well as on the Semiconductor material properties. For each meteorological condition there is a maximum power point (MPP) at which the system must work in order to deliver the optimal power to its load. The objective of the maximum power point trackers (MPPT) is to make the system work in this point or near. To track the maximum power a dc/dc converter is required with load voltage control. Dual converters are useful when dual output voltage levels are required from a single input supply voltage with MPPT. Fly back converter is capable to produce dual output voltage levels but it requires transformer. The gain of fly back converter is dependent on the turns ratio of transformer. Sefic converters used for step up and step down application [9]. High gain multilevel boost converter is used to step up the voltage level with large conversion ratio [10]. More number of switches and elements are required for generating dual output voltage level from conventional converters. Due to increases in number of switches and elements, conversercircuit becomes more expensive and complex [11].
II. PHOTOVOLTAIC MODELING

The simplest model of a PV cell consists of an ideal current source in parallel with an ideal diode as shown in Figure 1. The current source of PV cell represents the current generated by photons and its output is constant under constant temperature and constant incident radiation of light. A solar cell is the building block of a PV panel. A solar cell module is formed by connecting many solar cells in series and parallel. Considering only a single solar cell, it can be modeled by using a current source, a diode and two resistors. This model is known as a single diode model of a PV cell.

The output current from the PV cell is found by applying the Kirchoff’s current law on the equivalent circuit.

\[ I = I_{ph} - I_D \] (1)

Where \( I \) is the output current from PV cell, \( I_{ph} \) is the photon current, \( I_D \) is the diode current. The ideal diode equation is given as follows:

\[ I_D = I_S \left( e^{qV_d/kT} - 1 \right) \] (2)

Where \( I_D \) is the diode current, \( I_S \) is the saturation current, \( q \) is the electron charge, \( k \) is the Boltzmann constant and \( T \) is the actual temperature. By substituting Eq. 2 in Eq. 1, we get the value of the photon current \( I_{ph} \).

The photocurrent mainly depends on the solar insulation and cell’s working temperature, which is described as

\[ I_{ph} = \left[ I_{sc} + K_i(T-298) \right] \frac{\lambda}{1000} \] (3)

where \( I_{ph} \) is the photon current, \( I_{sc} \) is the cell’s short circuit current, \( K_i \) is the cell’s short-circuit current temperature coefficient, \( T \) is the solar cell’s actual temperature, and \( \lambda \) is the solar insulation. The reverse saturation current is expressed as

\[ I_{RS} = I_{sc}/[\exp(qV_{oc}/N_s kAT)-1] \] (4)

where \( I_{RS} \) is the reverse saturation current, \( V_{oc} \) is the open circuit voltage, \( N_s \) is the number of cells connected series, \( A \) is the ideality factor, \( k \) is the Boltzmann constant, \( q \) is the electron charge and \( T \) is the actual temperature.

The module saturation current \( I_s \) varies with the cell temperature, which is given by

\[ I_s = I_{RS} \left( \frac{T}{T_r} \right)^3 \exp \left( \frac{qE_g}{A kT} \left( \frac{1}{T_r} - \frac{1}{T} \right) \right) \] (5)

Where \( I_s \) is the saturation current, \( E_g \) is the band-gap energy of the semiconductor used in the cell, \( T_r \) is the reference temperature. The current output of PV module is

\[ I_p = N_p \left[ I_{ph} + I_{psh} \right] \left[ \exp \left( \frac{q(V_{oc}+I_{pp}R_s)}{A k T} \right) - 1 \right] \] (6)

Where \( I_{p} \) is the photovoltaic current and \( N_p \) is the number of cells connected in parallel. In fact, the PV efficiency is sensitive to small change in \( R_s \) but insensitive to variation in \( R_{sh} \). For a PV module, the series resistance becomes apparently important and the shunt resistance approaches infinity which is assumed to be open, where \( V_{pp}=V_{oc}, N_p=1 \) and \( N_s=36 \). The P-V and I-V curves of a solar cell are highly dependent on the solar irradiation values and temperature which is shown in Figure 2 and Figure 3.3. With increase in the solar irradiation the opencircuit voltage increases. Increase in temperature is accompanied by a decrease in the open circuit voltage value.

![Fig.1 Equivalent circuit of PV cell.](image1)

![Fig.2 I-V curve of a solar cell.](image2)
Increase in temperature causes increase in the band gap of the material and thus more energy is required to cross this barrier. Thus the efficiency of the photovoltaic cell is reduced.

III. MAXIMUM POWER POINT TRACKING

A typical solar panel converts only 30 to 40 percent of the incident solar irradiation into electrical energy. Maximum power point tracking technique is used to improve the efficiency of the solar panel. According to Maximum Power Transfer theorem, the power output of a circuit is maximum when the Thevenin impedance of the circuit (source impedance) matches with the load impedance. Hence our problem of tracking the maximum power point reduces to an impedance matching problem. In the source side we are using a self lift SEPIC converter connected to a solar panel in order to enhance the output voltage so that it can be used for different applications like motor load. By changing the duty cycle of the self lift SEPIC converter appropriately we can match the source impedance with that of the load impedance.

A. Incremental Conductance Algorithm

Incremental conductance method uses voltage and current sensors to sense the output voltage and current of the PV array. At MPP the slope of the PV curve is 0.

\[
\frac{dI}{dV} = -\frac{l}{V} \quad (\frac{dP}{dV} = 0)
\]  

(7)

The left hand side of the equation represents incremental conductance of the PV module, and the right hand side of the equation represents the instantaneous conductance of the PV panel. From the Equation 7, it is obvious that when the ratio of the change in the output conductance is equal to the negative output conductance, then maximum power point is reached.

\[
\frac{dI}{dV} > -\frac{l}{V} \quad (\frac{dP}{dV} > 0)
\]

(8)

\[
\frac{dI}{dV} < -\frac{l}{V} \quad (\frac{dP}{dV} < 0)
\]

(9)

Equation 8 and Equation 9 are used to determine the direction in which a perturbation must occur to move the operating point toward the maximum power point, and the perturbation is repeated until Equation 7 is satisfied. Once the MPP is attained, the MPPT continues to operate at this point until a change in current is measured. The present value and the previous value of the PV voltage and current are used to calculate the values of dI and dV. If dV>0 and dI>0, then the amount of sunlight has increased, by increasing the MPP voltage. Figure 4 shows the flowchart for the incremental conductance algorithm. Here we will measure both the voltage and current simultaneously. Hence the error due to change in insulation is eliminated. IncCon method is the simplest method when comparing to other MPPT methods.

Incremental Conductance method is the best methods because it does not produce steady state oscillations and it provides precise control under rapidly vary atmospheric condition. It can track the maximum power from the sun.
IV. SELECTING PROPER CONVERTER

There are a number of different topologies for DC-DC converters. The buck topology is used to step down the voltage. The boost topology is used for stepping up the voltage. Then, there are topologies able to step up and down the voltage such as: buck-boost, cuk converter and SEPIC converter. Thus, the additional boost capability can slightly increase the overall efficiency. The SEPIC and the self lift SEPIC converter can be able to step up and step down the voltage. Figure.5 shows the circuit diagram of SEPIC converter. Figure.6 shows the electrical circuit of self lift SEPIC converter.

A. SEPIC Converter

The Single Ended Primary Inductance Converter (SEPIC) is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. The capacitor C is used to transfer the energy and it is connected alternately to the input and to the output of the converter via the commutation of the transistor and the diode.

The maximum voltage obtained from the panel is unregulated. The unregulated voltage can be converted to regulated voltage by using a self lift SEPIC converter. Self lift SEPIC converter is one of the types of voltage lift converters. It is the improved version of SEPIC converter. In this converter the input current and the output current is continuous. The output voltage ripple produced in this converter is very less when compared to SEPIC converter.

As for component stress, it can be seen that the self lift SEPIC converter has smaller voltage and current stresses than the SEPIC converter. It has low switching losses and highest efficiency when compared to SEPIC converter. Figure.6 shows the self lift SEPI converter equivalent circuit. Figure.7 and Figure.8 shows its operating modes, which acts like an interface between PV panel and the resistive load.

B. Operating Modes of Self Lift SEPI Converter

This converter performs DC-DC voltage increasing conversion in simple structure. The self lift SEPI converter has two modes of operation.

1) Mode 1: During the first mode of operation the switch will be turned on. The switch S, D1 are on and diode D is off. During switch-on period, the voltage across the capacitors C and C1 are equal.

The equations for the switch conduction mode are as follows:

\[ V_{c1} = V_c = V_1 \]  
\[ V_0 = V_{c2} = V_{c0} \]

In steady state, the average voltage across inductor \( L_0 \) over a period is also zero.

Thus,

\[ kTV_1 = (1-k)T (V_c - V_{c1} + V_{c2} - V_1) \] 

and hence

\[ V_0 = V_{c2} = V_{c0} = \frac{V_1}{(1-k)} \]

Since all the components are ideal, the power loss associated with all the circuit elements is neglected. Therefore the output power \( P_o \) is considered to be equal to the input power \( P_{IN} \):
2) Mode 2: During the switch-off condition, diode D is on, switch S and diode D1 are off. The inductor current decreases and diode D is forward biased and the capacitor C is charged by using the input supply. The capacitor C acts as a low pass filter so that

\[ I_{L0} = I_0 \]  

The current \( i_L \) increases during switch-on. The voltage across it during switch-on is \( V_1 \), therefore its peak to peak current variation is

\[ \Delta i_L = \frac{kV_0}{L} \]  

During the steady state condition the average inductor voltage and the capacitive current waveforms are zero. The relationship between the output and input currents are given in the following:

\[ \frac{i_1}{I_0} = \frac{1}{1-k} \]  

The peak to peak variation of the voltage \( V_c \) is

\[ \Delta V_c = \frac{I_0}{fC} \]  

Assuming 5% of ripple in capacitor voltage \( \Delta V_{c1} \), we can find the value of \( C1 \). The peak to peak variation of the voltage \( V_{c2} \) is

\[ \Delta i_{L0} = \frac{kV_0}{8f^2L_0C_2} \]  

Assuming 5% of ripple in the inductor current, we can find the value of \( L_0 \). The peak to peak variation of voltage \( V_0 \) and \( V_{c0} \) is

\[ \Delta V_0 = \Delta V_{c0} = \frac{I_0k}{64f^3L_0C_2C_0} \]  

Assuming 5% of ripple in capacitor voltage \( \Delta V_{c0} \) we can find the value of filter capacitor \( C_0 \).

**V. DIODE-CLAMP MULTILEVEL INVERTER**

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is \( V_{dc} \). An \( n \)-level inverter needs \( (n-1) \) voltage sources, \( 2(n-1) \) switching devices and \( (n-1)(n-2) \) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform.
C₃ and C₄. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes. The order of numbering of the switches for phase a is S1, S2, S3, S4, S1’, S2’, S3’ and S4’. For example to have Vdc/2 in the output, switches S1 to S4 should conduct at the same time. For each voltage level four switches should conduct. As it can be seen in Table 1, the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. The output voltage of a 5-level diode clamped multilevel inverter all of the voltage level should have the same voltage value. The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this thesis is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles. Table 1 shows the output voltage levels and the corresponding switch states for one phase of the chosen five-level DCMLI. The switches are arranged into 4 pairs (S1, S1’), (S2, S2’), (S3, S3’), (S4, S4’). If switching sequence as given in table 1. State condition 1 means switch ON and 0 means switch OFF.

Table 1: The switching state of diode clamp multilevel inverter.

<table>
<thead>
<tr>
<th>V₀</th>
<th>S₁</th>
<th>S₂</th>
<th>S₃</th>
<th>S₄</th>
<th>S₁’</th>
<th>S₂’</th>
<th>S₃’</th>
<th>S₄’</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdc/2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Vdc/4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-Vdc/4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>-Vdc/2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The steps to synthesis the five level phase a output voltage in this work are as follows:
1. For phase a output voltage of Van=0, two upper switches S3, S4 and two lower switches S1’ and S2’ are turned on.
2. For an output voltage of Van=Vdc/4, three upper switches S2, S3, S4 and one lower switch S1’ are turned on.
3. For an output voltage of Van=Vdc/2, all upper switches S1 through S4 are turned on.
4. To obtain the output voltage of Van= -Vdc/4, upper switch S4 and three lower switches S1’, S2’ and S3’ are turned on.
5. For an output voltage of Van = -Vdc/2, all lower switches S1’ through S4’ are turned on.

The phase a output voltage Van has five states: Vdc/2, Vdc/4, 0, -Vdc/4 and -Vdc/2. The gate signals for the chosen five-level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices.

VI. MATLAB/SIMULATION RESULTS

Fig. 10. Simulink model of the PV panel connected to the SEPIC converter with MPPT.

Fig. 11. Simulation results of PV panel connected to the SEPIC converter with MPPT.

Fig. 12. Simulink model of the PV panel connected to the self lift SEPIC converter with MPPT.
Fig.13. Simulation results of PV panel connected to the self lift SEPIC converter with MPPT.

Fig.14. Simulink model of the PV panel connected to the self lift SEPIC converter with MPPT and single phase five level inverter.

Fig.15. Output Voltage of five level inverter.

VII. CONCLUSION

This paper proposes a simple MPPT method that requires only measurements of voltage and current. The proposed Incremental conductance MPPT algorithm increases the efficiency and it tracks the maximum power from the sun. This method computes the maximum power and controls directly the extracted power from the PV by changing the duty cycle in the self lift SEPIC converter. This method computes the maximum power and controls directly the extracted power from the PV by changing the duty cycle in the Multi level SEPIC converter. The voltage produced by High Gain Multi level SEPIC converter is higher when compared to Self lift SEPIC converter. The proposed method offers different advantages which are: good tracking efficiency, response is high and well control for the extracted power and also for load voltage control.

REFERENCES